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10/799,461	03/12/2004	Brian Gerard Goodman	TUC920040001US1	7713

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EXAMINER	
KARIMI, PEGEMAN	

ART UNIT	PAPER NUMBER
2609	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/799,461	GOODMAN ET AL.	
	Examiner	Art Unit	
	Pegeman Karimi	2609	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *03/12/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 101

1. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 31-39 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims 31-39 recites "a computer program product"; however, claims 31-39 neither include any computer hardware component(s) nor positively recite that the cited software programs are useable with a processor of an electronic device. As such claims 31-39 are directed toward software per se, which is non-functional descriptive material and non-statutory.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-44 rejected under 35 U.S.C. 102(b) as being anticipated by Kayser (U.S. Patent 6,089,453).

As to claim 1, Kayser discloses an electronic device (20), comprising:

a nonvolatile memory (Fig. 19a, 150) for storing information regarding said electronic device (col. 33, lines 17-20);

an electronic persistent visual display (156) having an input (C, conductor),

said electronic persistent visual display providing a visual label display (Fig. 17a, 317) which persists indefinitely (The information on the label can be changed see Fig. 18b), until updated by an input signal at said input (col. 12, lines 12-18 and col. 68, lines 55-61);

at least one operational element (158); and

a processor (146) for operating said at least one operational element (col. 66, lines 21-23);

said processor, in response to a predetermined state (start-up), providing an update input signal (Product information) at said electronic persistent visual display input (20),

said update input signal comprising selected said information regarding said electronic device stored in said nonvolatile memory (software initialization, col. 13, lines 37-42 and col. 69, lines 35-41),

said update signal to update said visual label display of said electronic persistent visual display (col. 12, lines 12-14).

As to claim 15, this claim differs from claim 1 only in that the limitations "stored by said processor" is additionally recited. Kayser teaches the processor stores the display tag address (col. 66, lines 38-43).

As to claim 31, this claim differs from claim 1 only in that the limitation " A computer program" is additionally recited. Kayser teaches a computer program product (program ROM, 2064) usable with a processor (2003) of an electronic device (ASIC, 2001), said computer program product having computer readable program code embodied therein for operating at least one operational element (col. 49, lines 18-20).

As to claim 40, this claim differs from claim 1 only in that the limitation states " a Network and a network interface" Kayser teaches a system (Fig. 2) comprising:

a network (communication network, 27) ;

and a plurality of components (20), at least one of said components comprising:

a network interface (31) to said network (27);

As to claims 2, 16, 32, and 41, Kayser teaches the predetermined state (start-up) of said processor comprises a power-on and/or reset of said processor (col. 26, lines 59-60) .

As to claims 3, 17, and 33, Kayser teaches the processor additionally updates said information regarding said electronic device stored in said nonvolatile memory (col. 68, lines 40-44), and said processor update signal selected information (received address) comprises at least said updated information (information data) regarding said electronic device (col. 68, lines 44-46).

As to claims 4, 18, and 34, Kayser teaches the processor comprises a programmable computer processor (col. 68, lines 63-67) and said predetermined state (Power-on self-test) of said processor comprises completion of an update to computer readable program code (displaying the received data packet) of said programmable computer processor (col. 69, lines 14-19).

As to claims 5, 19, and 35, Kayser teaches the processor (146) additionally updates said information regarding said electronic device stored in said nonvolatile memory (col. 68, lines 37-46) with status information (new look up table) related to said update to computer readable program code of said programmable computer processor (col. 26, lines 46-56), and said processor update signal selected information comprises at least said status information (col. 26, lines 46-49).

As to claims 6 and 20, Kayser teaches the processor comprises programmable logic (Display driver, 158) and said predetermined state of said processor comprises completion of an update to said programmable logic (252, col. 69, lines 17-19).

As to claims 7 and 21, Kayser teaches the processor additionally updates said information regarding said electronic device stored in said nonvolatile memory (col. 26,

lines 46-50) with status information related to said update to said programmable logic (new display tag to be added), and said processor update signal selected information (look-up table) comprises at least said status information (col. 26, lines 52-56).

As to claims 8 and 22, Kayser teaches the predetermined state of said processor comprises a state achieved (steps 1344 through 1347, Fig. 13e) in response to an indication of completion (new display tag) of an engineering change to said electronic device (Adding a display tag, col. 27, lines 39-41 and lines 55-57).

As to claims 9,11, 23, 25, 36, and 38, Kayser teaches the processor additionally updates said information regarding said electronic device stored in said nonvolatile memory (col. 68, lines 37-43) with status information related to said engineering change to said electronic device (1344, Fig. 13e), and said processor update signal selected information comprises at least said status information (col. 68, lines 40-46).

As to claims 10, 24, 37, and 42, Kayser teaches the predetermined state of said processor comprises a state achieved (steps 1344 through 1347) in response to an indication of a change to said at least one operational element (New tag setup, col. 27, lines 55-57).

As to claims 12 and 26, Kayser teaches the electronic device additionally comprises an input/output interface (31); and

said predetermined state of said processor (Start-up mode) comprises a state achieved in response to a signal received at said input/output interface (col. 18, lines 1-7 & col. 68, lines 40-51).

As to claims 13, 27, and 43, Kayser teaches the processor additionally selects (address which matches its stored address) said information stored in said nonvolatile memory in accordance with said signal received at said input/output interface (col. 68, lines 40-46 & col. 18 lines 1-7).

As to claims 14, 30, 39and 39, Kayser teaches the predetermined state (reset) of said processor comprises an expiration of a predetermined interval of time (col. 48, lines 49-53).

As to claim 28, Kayser teaches the electronic device comprises a component for a system (28, Fig. 2), said system comprising a network coupling said electronic device (31) within said system (col. 12, lines 52-53), and

wherein said electronic device additionally comprises a network interface to said network (col. 12, lines 47-50); and

said predetermined state (start-up mode) of said processor comprises a state achieved in response to a signal received at said network interface (col. 68, lines 47-53).

As to claim 29, Kayser teaches the processor additionally selects said information stored by said processor (stored address) in accordance with said signal received at said network interface (col. 68, lines 40-46).

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Briechle et al. (U.S. Patent 5,632,010) discloses a technique for communicating with electronic labels in an electronic price display system.

Revesz et al. (U.S. Patent 4,962,466) discloses an electronic product information display system.

Inquiries

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pegeman Karimi whose telephone number is (571) 270-1712. The examiner can normally be reached on Monday-Thursday 8:00am - 5:00pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chanh Nguyen can be reached on (571) 272-7772. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Pegeman Karimi
04/23/2007

CHANH D. NGUYEN
SUPERVISORY PATENT EXAMINER